VLSI Project: Elevator Control System

Part 5

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H/W: 10.147 by 4.306

Tsu\_dd = 0.00736 ns

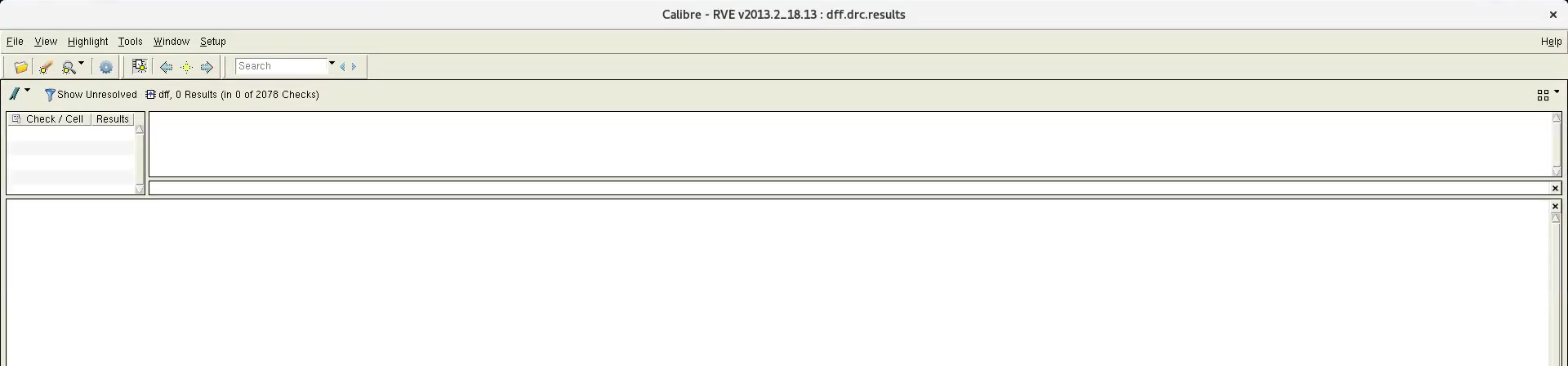
Tsu\_opt = 0.0 ns

Td = 0.179 ns

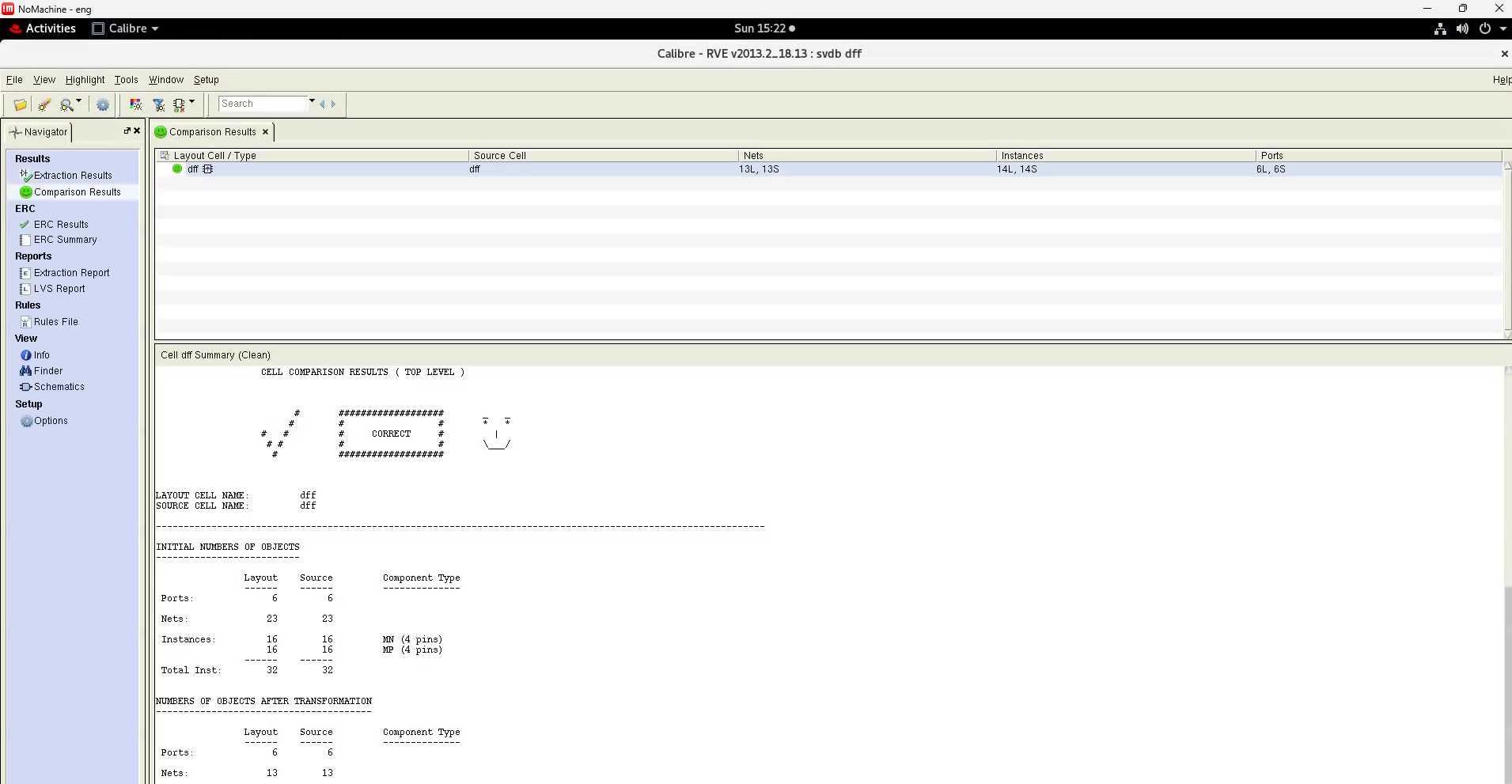
Tck->Q = 0.179 ns

Thold = -0.00001 ns

**DFF DRC Screenshot**

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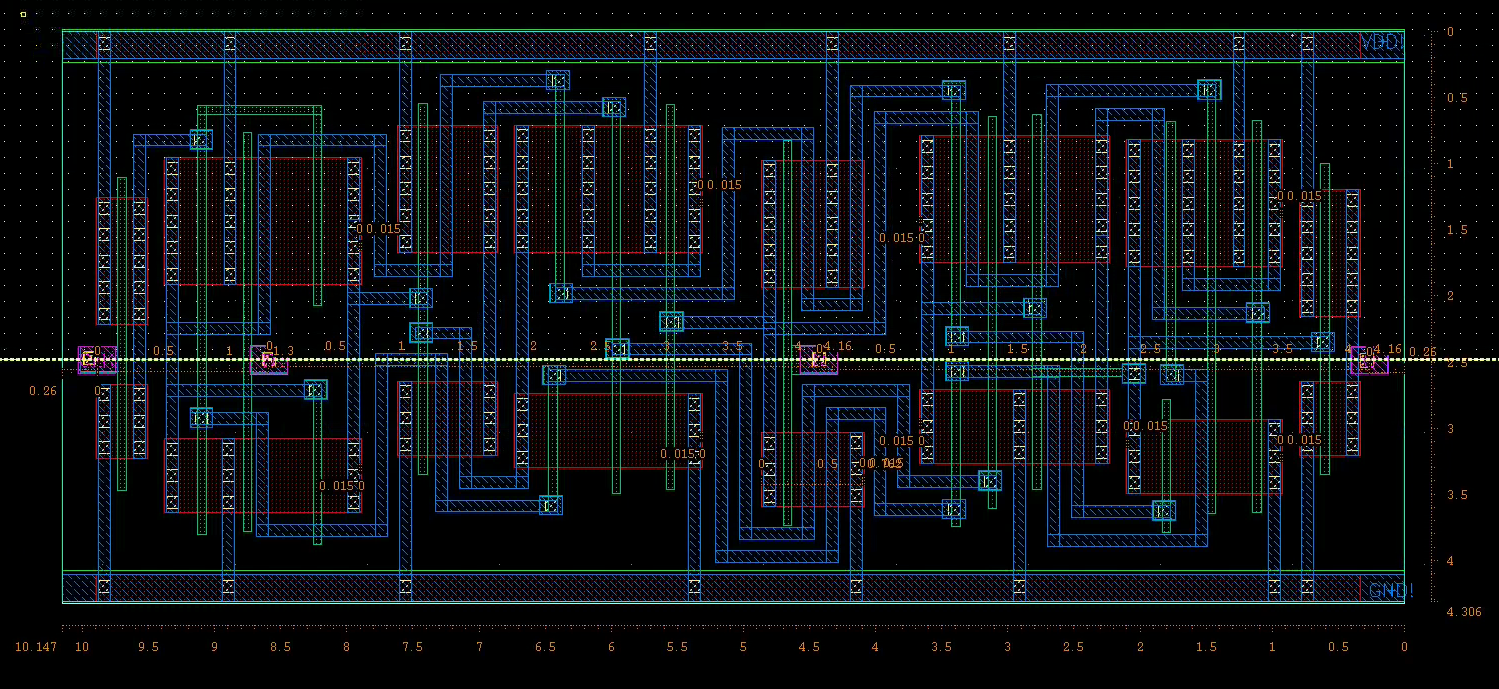
**DFF LVS Screenshot**



**Cell Height & Width Screenshot**

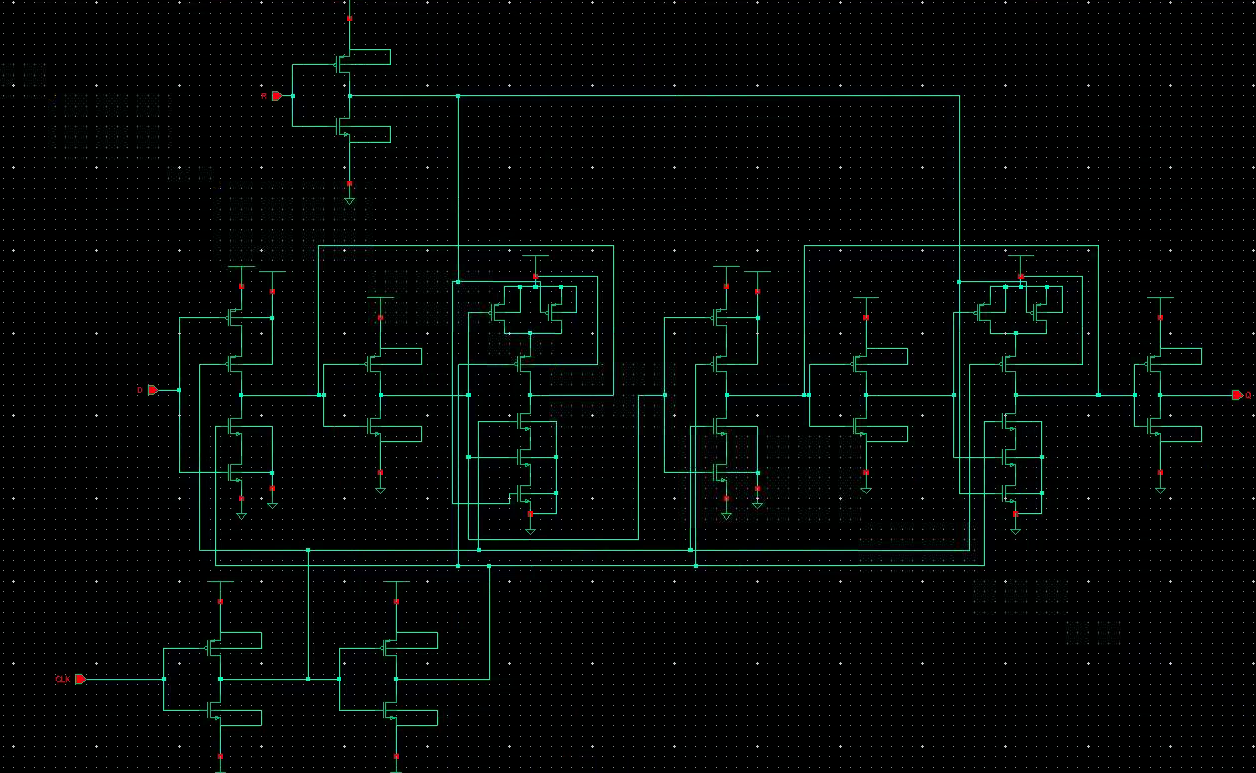


**DFF Layout Screenshot**

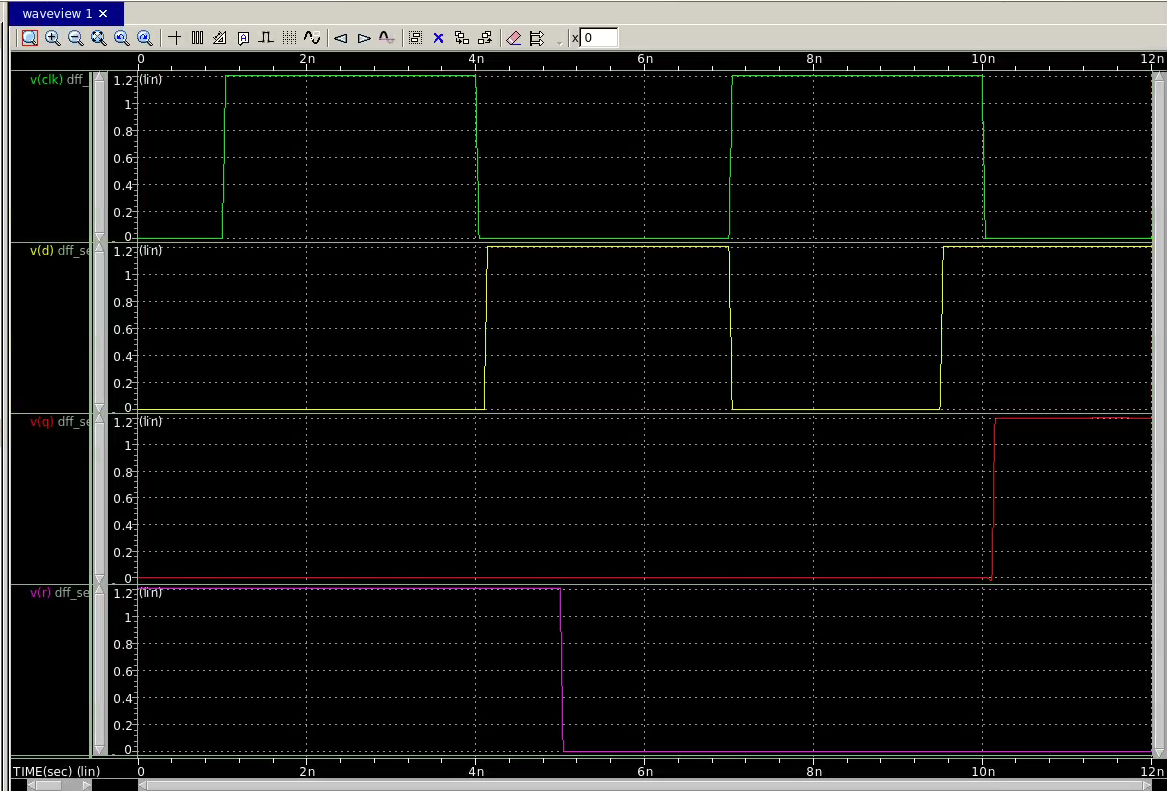


Note: Pin pitch = INTEGER MULTIPLE of 0.26

**DFF Schematic Screenshot**



**DFF Output Check Waveform Screenshot**



**DFF Drop Dead Waveform Screenshot**



**DFF Timing Results**

Tsu\_dd = 0.00736 ns

Tsu\_opt = 0.00000 ns (D is high exactly at the falling edge of the clock)

Td = 0.179 ns

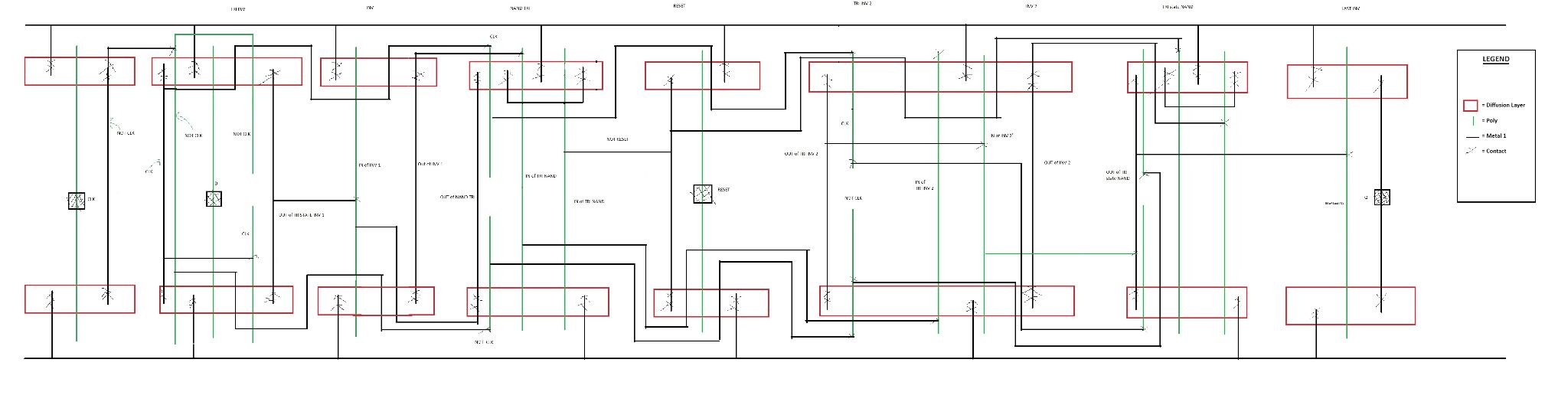
Tck->Q = 0.179 ns

Thold = -0.00001 ns (one step size diff between Tsu\_dd)

**DFF Time Attribute Gathering Explanation**

The way we found the various flip-flop times was by manually running each sweep till the resulting Q would not go to the high value. We ran each pulse on D separately and narrowed down the value of the drop dead, where the Q value does not rise despite D high and R low. This was shown to be 0.00736 ns after the falling edge of the clock. To find Tsu\_opt we used a DC sweep to find the minimum time from D to Q (50% to 50%) and the time that has the minimum time is Tsu\_opt, which was 0 for us. Td for Tsu\_opt was equal to the time from D to Q (50% to 50%).

**DFF Layout Sketch**



**DFF Layout Sketch Explanation**

Due to the limitations of no metal2 and limited amounts of horizontal poly, we decided to wire almost all of the gates with metal1 (only 2 are wired with short horizontal polys). The layout was designed with a greedy method from left to right. This means that for each gate, we do not care about future wires and only care about the wires to itself and past gates. We chose this method because it was the simplest layout to design by hand, with the tradeoff of optimal size.